Notice of Allowability	Application No.	Applicant(s)	
	10/656,049	SAITO, KYOZO	
	Examiner	Art Unit	
	Phillip Nguyen	2828	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *8/22/05*.

2. ☒ The allowed claim(s) is/are *3-8*.

3. ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☒ All b) ☐ Some* c) ☐ None of the:
      1. ☒ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____.
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

4. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

5. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

6. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☒ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date 9/5/03
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☒ Interview Summary (PTO-413), Paper No./Mail Date *9/1/05*.
7. ☒ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

EXAMINER'S AMENDMENT

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

Authorization for this examiner's amendment was given in a telephone interview with Anthony Curtis on 9/1/05.

2. The application has been amended as follows:

In the specification:

Page 8, line 20: delete "21B" and insert --21b--

Page 9, lines 23-24: delete "K U" and insert --kΩ--

Page 11, lines 15-16, delete "U", "kU" and "U", insert --Ω--, --kΩ-- and --Ω--, respectively.

In the claims:

Please amend the claims as follows:

3. (Currently Amended) An optical output control circuit of a semiconductor laser comprising:

the semiconductor laser ~~for supplying~~receiving a modulating electric current and a bias electric current ~~therete~~;

modulating electric current supplying means for supplying said modulating electric current on the basis of an inputted modulating signal; and

bias electric current supplying means for supplying said bias electric current,

wherein first temperature correcting means for increasing said modulating electric current with a rise in ambient temperature is arranged in said modulating electric current supplying means,

a second temperature correcting ~~circuit~~ means for increasing said bias electric current with said rise in ambient temperature is arranged in said bias electric current supplying means,

a feedback circuit negatively fed back by said bias electric current is arranged in said bias electric current supplying means,

said first temperature correcting means is constructed by a first resistor circuit constructed by a first thermistor, a first resistor connected in series to said first thermistor, and a second resistor connected in parallel to said first thermistor, and is also constructed by a third resistor connected in series to said first resistor circuit,

said second temperature correcting means is constructed by a second resistor circuit constructed by a second thermistor, a fourth resistor connected in series to said second thermistor, and a fifth resistor connected in parallel to said second thermistor, and is also constructed by a sixth resistor connected in series to said second resistor circuit,

said modulating signal is inputted between both terminals of said first temperature correcting means,

a direct current voltage is applied between both terminals of said second temperature correcting means,

said modulating electric current is supplied by the modulating signal outputted between ~~both ends of~~ said third resistor and the first resistor circuit, and

said bias electric current is supplied by a divided voltage outputted between ~~both ends of~~ said sixth resistor and the second resistor circuit.

4. (Currently Amended) An optical output control circuit of a semiconductor laser comprising:

the semiconductor laser ~~for supplying~~receiving a modulating electric current and a bias electric current ~~thereto~~;

modulating electric current supplying means for supplying said modulating electric current on the basis of an inputted modulating signal; and

bias electric current supplying means for supplying said bias electric current,

wherein first temperature correcting means for increasing said modulating electric current with a rise in ambient temperature is arranged in said modulating electric current supplying means,

a second temperature correcting means ~~circuit~~ for increasing said bias electric current with said rise in ambient temperature is arranged in said bias electric current supplying means,

a feedback circuit negatively fed back by said bias electric current is arranged in said bias electric current supplying means,

said feedback circuit is constructed by a transistor for flowing said bias electric current to said semiconductor laser, a seventh resistor connected between an emitter of said transistor and ground, and an operational amplifier interposed between said second temperature correcting means and a base of said transistor, and a divided voltage is applied to a non-inversion input terminal of said operational amplifier, and the emitter of said transistor is connected to an inversion input terminal of said operational amplifier.

5. (Currently Amended) The optical output control circuit of the semiconductor laser according to claim 4, wherein:

said first temperature correcting means is constructed by a first resistor circuit constructed by a first thermistor, a first resistor connected in series to said first thermistor, and a second resistor connected in parallel to said first thermistor, and is also constructed by a third resistor connected in series to said first resistor circuit,

said second temperature correcting means is constructed by a second resistor circuit constructed by a second thermistor, a fourth resistor connected in series to said second thermistor, and a fifth resistor connected in parallel to said second thermistor, and is also constructed by a sixth resistor connected in series to said second resistor circuit,

said modulating signal is inputted between both terminals of said first temperature correcting means,

a direct current voltage is applied between both terminals of said second temperature correcting means,

said modulating electric current is supplied by the modulating signal outputted between ~~both ends of~~ said third resistor and the first resistor circuit, and

said bias electric current is supplied by a divided voltage outputted between ~~both ends of~~ said sixth resistor and the second resistor circuit.

6. (Currently Amended) An output control circuit comprising:

a modulating electric current supplier configured to receive a modulating signal and supply a modulating electric current, the modulating electric current supplier containing a first temperature corrector that increases the modulating electric current as an ambient temperature rises; and

a bias electric current supplier that supplies a bias electric current, the bias electric current supplier containing a second temperature corrector that increases the bias electric current as the ambient temperature rises,

wherein the first temperature corrector has a first resistor circuit and a first resistor connected in series to the first resistor circuit, the first resistor circuit includes a first thermistor, a second resistor connected in series to the first thermistor, and a third resistor connected in parallel to the first thermistor, the modulating signal is supplied to an input between terminals of the first temperature corrector, the modulating electric current is supplied by a modulating signal provided to an output between ends of the first resistor, and

the second temperature corrector has a second resistor circuit and a fourth resistor connected in series to the second resistor circuit, the second

resistor circuit includes a second thermistor, a fifth resistor connected in series to the second thermistor, and a sixth resistor connected in parallel to the second thermistor, a direct current voltage is applied between terminals of the second temperature corrector, the bias electric current is supplied by a divided voltage provided to an output between ~~ends of~~ the fourth resistor and the first resistor circuit.

8. (Currently Amended) The output control circuit of Claim 7, wherein:

the first temperature corrector has a first resistor circuit and a second resistor connected in series to the first resistor circuit, the first resistor circuit includes a first thermistor, a third resistor connected in series to the first thermistor, and a fourth resistor connected in parallel to the first thermistor, the modulating signal is supplied to an input between terminals of the first temperature corrector, the modulating electric current is supplied by a modulating signal provided to an output between ends of the second resistor, and

the second temperature corrector has a second resistor circuit and a fifth resistor connected in series to the third resistor circuit, the second resistor circuit includes a second thermistor, a sixth resistor connected in series to the second thermistor, and a seventh resistor connected in parallel to the second thermistor, a direct current voltage is applied between terminals of the second temperature corrector, the bias electric current is supplied by a divided voltage provided to an output between ~~ends of~~ the fifth resistor and the second resistor circuit.

Allowable Subject Matter

3. The following is an examiner's statement of reasons for allowance: Claims 3-8 are allowed because the prior art fail to teach or fairly suggest an output control circuit (driver circuit) of a semiconductor laser as cited in the claims especially with two temperature correcting means each supplies to the inputs of current modulation and bias circuits feeding the laser wherein the temperature correcting means comprises resistors connected in series and parallel with the thermistor and providing output at the connection between of series and parallel resistors.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Communication Information

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Phillip Nguyen whose telephone number is 571-272-1947. The examiner can normally be reached on 9:00 AM - 6:00 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, MINSUN HARVEY, can be reached on 571-272-1835. The fax phone number for the organization where this application or proceeding is assigned is **571-273-8300**.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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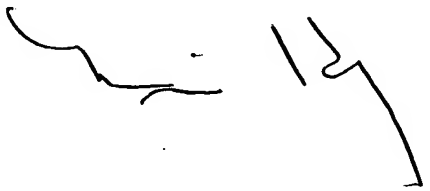

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PRIMARY EXAMINER